REMARKS/ARGUMENTS

Claims 1-14 are pending. Claim 14 has been appended.

Claims 1, 2, 6, 7, and 9-12 were rejected under 35 U.S.C. 102(e) for allegedly being anticipated by Dupuy et al.

Claims 1, 3-5 and 8 were rejected under 35 U.S.C. 102(b) for allegedly being anticipated by Tsunoda et al.

Claims 1 and 13 are rejected under 35 U.S.C. 102(e) for allegedly being anticipated by Shukuri et al.

Distinguishing aspects of the present invention as recited in the pending claims include identifying first, second, and third regions in an active region of a semiconductor die. The first, second, and third regions comprise, respectively, first, second, and third active cells fabricated according to respective first, second, and third cell designs. The resulting first active cells are different from the second active cells, and the third active cells are different from the second and third active cells.

The reference to Dupuy et al. shows in Fig. 4 an array transistors that is partitioned into sub-arrays (41, 42, 43) with bonding pads (45, 46, 47) interspersed amongst the sub-arrays. Fig. 9 shows lateral FET-type transistors in a portion (101) surrounded by transistor portions (102, 103, 104, 105). The transistors in portion (101) conduct less current. *Col. 6, lines 30-31.* Fig. 10 show a similar arrangement of transistors as shown in Fig. 9, but for vertical FET-type transistors. Dupuy et al., however, do not show or suggest the recited first, second, and third regions with their respective first, second, and third active cell designs.

The Tsunoda et al. reference shows in Figs. 3A and 3B views of an IGBT having a current sensing function. See generally column 4, line 66 to column 5, line 25. They show a principal current cell region (21) and a current sensing cell region (22). However, they do not show or suggest a third cell region having active cells different from either the principal current cells or the current sensing cells. Tsunoda et al. neither teach nor suggest the present invention as recited in the pending claims.

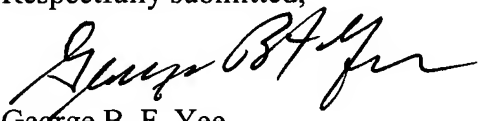
The Shukuri et al. reference is directed to a microprocessor design. They show a DRAM (106) about which are disposed arrays of flash memory cells (113, 114, 115). Each flash memory cell comprises a non-volatile memory cell (131) including a pair of nonvolatile memory elements (130). See Figs. 3 - 6. Shukuri et al. do not show or suggest a third cell region having active cells different from either the DRAM cells or the flash memory cells. Tsunoda et al. neither teach nor suggest the present invention as recited in the pending claims.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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